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PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

September 25, 2007 — Date

Alexandra Beggs

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Tae H. Kim	Attorney Docket No.:	501299.01
Patent No.	: US 6,975,552 B2	Serial No.	: 10/644,610
Issue Date	: December 13, 2005	Filed	: August 19, 2003
Title	: HYBRID OPEN AND FOLDED DIGIT LINE ARCHITECTURE		

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line	Reads	Should Read
Item (57), Line 3	"and an open digit line"	--and open digit line--
Column 1, Lines 45, 50 and 52	"complimentary"	--complementary--
Column 2, Line 40	"pair is surrounded"	--pair being surrounded--
Column 4, Line 30	"to which portion of a digit line memory cells are"	--to which portions of a digit line of memory cells are--
Column 4, Line 41	"aspects of a open digit line"	--aspects of an open digit line--

Column 4, Line 64	"array **10**, thus, coupling"	--array **10**, thus coupling--
Column 5, Line 57	"memory arrays, thus,"	--memory arrays, thus--
Column 5, Line 59	"to active column **50, 80**"	--to active columns **50, 80**--
Column 6, Line 27	"but are instead, shifted"	--but are instead shifted--
Column 6, Line 41	"are desired. For example,"	--are desired; for example,--
Column 6, Line 66	"MDL portion **156**. virtue of the data state stored by the"	--MDL portion **156**. Consequently, the voltage of the digit line will be altered from the precharge voltage by virtue of the data state stored by the--
Column 7, Line 38	"of the memory arrays **202***a*, **202***b* is a respective row various"	--of the memory arrays **202***a*, **202***b* is a respective row address latch **226**, which stores the row address, and a row decoder **228,** which applies various--
Column 14, Line 21	"cells of the colunm"	--cells of the column--

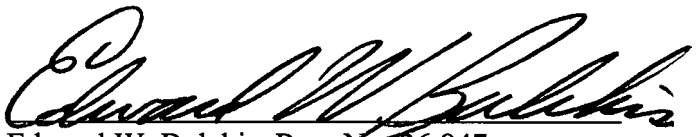
The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: September 24, 2007

By: 

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Enclosures:
Postcard
Form PTO-1050 (+ copy)

501299.01 req cert correct

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : US 6,975,552 B2
DATED : December 13, 2005
INVENTOR(S) : Tae H. Kim

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